fine power®

600W LLC converter with digital control

Software Documentation

Matthias Tauer

RELEASED

Issue: 1.0.0

Scope

The purpose of this document is to provide a regularly updated software documentation during the design process of the digital control software algorithms.

This document is a living document. It will be initially established during the requirements phase and updated during the design, implementation and integration phase.

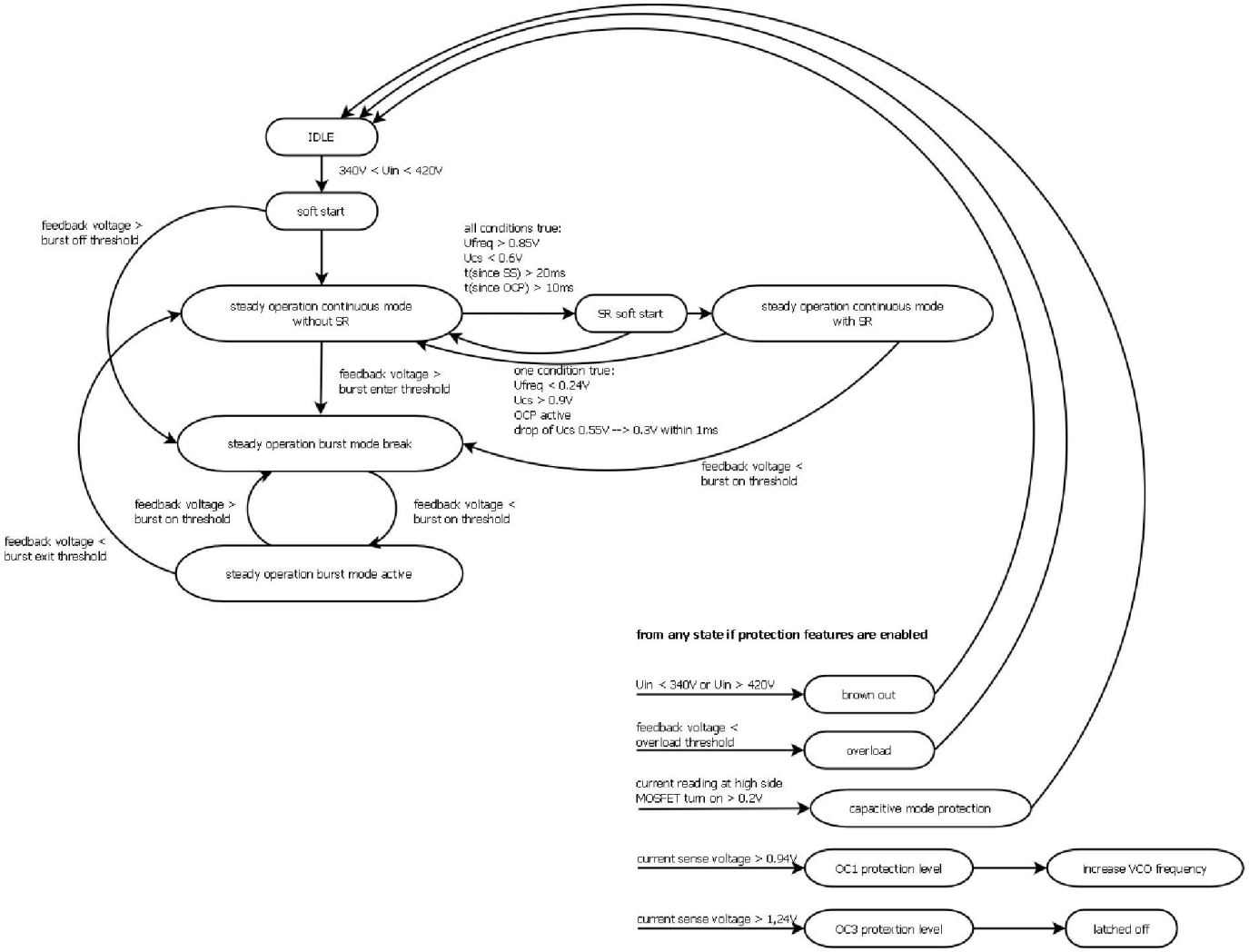
Until final release of this document the content is to be regarded as preliminary.

Released version will be indicated on first slide as released.

Summary

- The digital control module is a one to one replaceable for the analog control module
- The digital control module reflects the same functions than the analog control IC (according to the datasheet of ICE2HS01G)
- Additional functions can be implemented in the digital control as follows:
  - Adaptive dead time control
  - Improved turn-on/off behavior of SR
  - Improved dynamic response
  - Prevention of capacitive mode operation
- The digital control will **not** provide:
  - Full digital control loop with the possibility to place poles and zeros

State Machine



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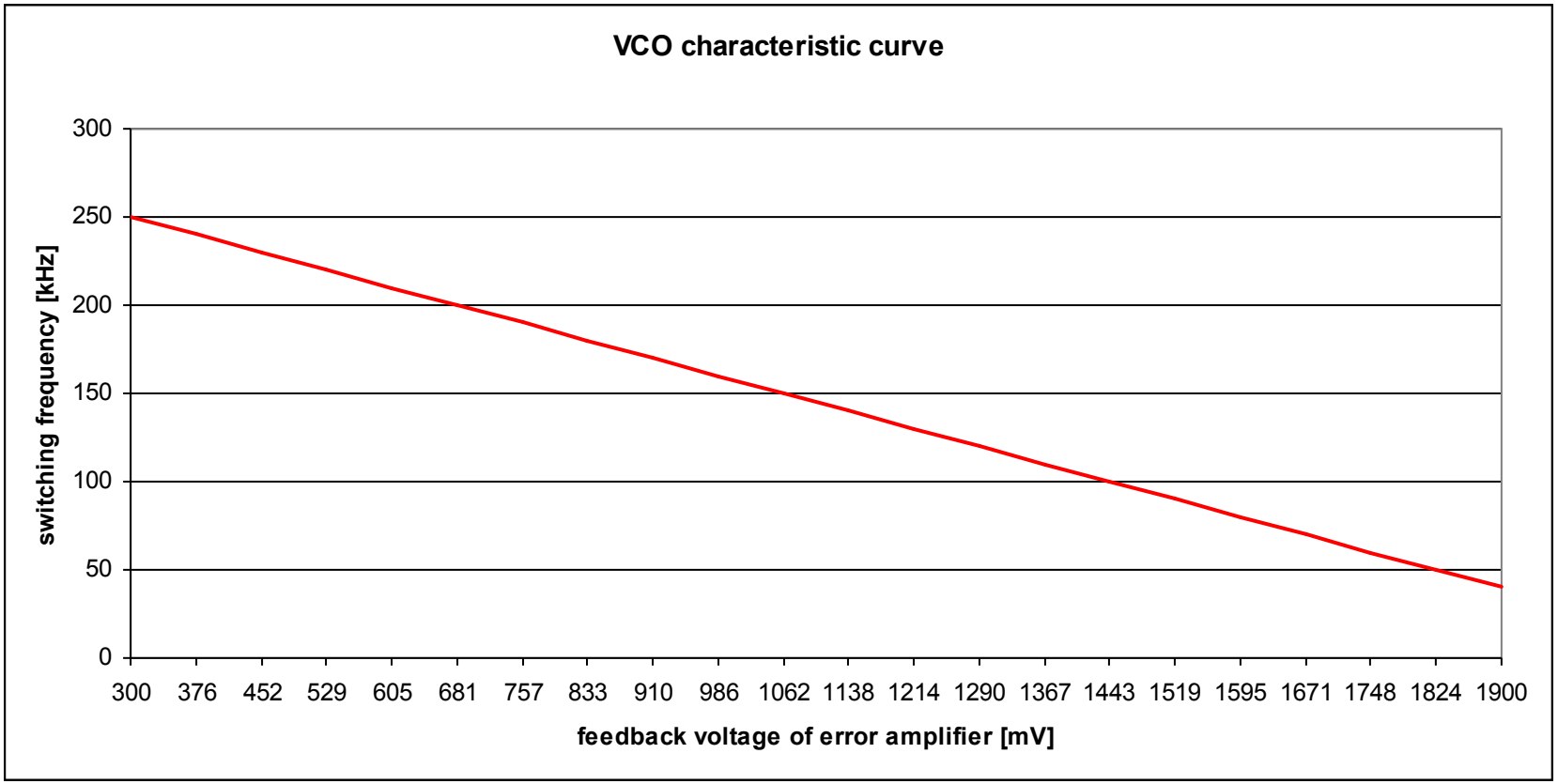
Functional Description

Feature	Concept of implementation	Realized implementation	Remark
Soft-start	1) $f_{sw} = f_{max}$, duty cycle = 0% 2) $f_{sw} = f_{max}$, increase duty cycle to 100% 3) Sweeping f_{sw} down until control loop takes over	•$f_{sw} = f_{max}$ •Sweeping f_{sw} down until control loop takes over	•During Soft-start the OCP threshold is increased for 500us •SR is disabled during soft-start • 20ms after soft-start is finished SR is enabled
Over-current protection	Two-level over current protection: • Ucs > 0.94V: increase of f_{sw} • Ucs > 1.24V: stop PWM, latched off	Two-level over current protection: • Ucs > 0.94V: increase of f_{sw} • Ucs > 1.24V: stop PWM, latched off	• OCP is done with analog to digital comparator • SR is turned off if $U_{cs} > 0.82V$ •SR is turned on again if $U_{cs} < 0.54V$
Burst Mode (BM)	Feedback voltage of error amplifier is monitored: Entering BM: $U_{freq} < 0.38V$, (f_{sw} = 245kHz) Leaving BM: $U_{freq} > 0.45V$, (f_{sw} = 230kHz) • For preventing hard commutation the duty cycle during BM is limited to 25%. • After leaving BM duty cycle is increased linear from 25% to 100%.	Feedback voltage of error amplifier is monitored: Entering BM: $U_{freq} < 0.38V$, (f_{sw} = 245kHz) Leaving BM: $U_{freq} > 0.45V$, (f_{sw} = 230kHz) • No duty cycle reduction during BM or when leaving BM	•SR is disabled during BM.
Over load and open loop protection	Feedback voltage of error amplifier is monitored: If $U_{freq} > 1.861V$ PWM is stopped. After $t_{restart}$ a soft-start is initiated.	Feedback voltage of error amplifier is monitored: If $U_{freq} > 1.861V$ PWM is stopped. After $t_{restart}$ a soft-start is initiated.	
Brown-out protection	Input voltage is monitored: •340V < V_{in} < 420V: normal operation •V_{in} < 340V or V_{in} > 420V: no operation	Input voltage is monitored: •340V < V_{in} < 420V: normal operation •V_{in} < 340V or V_{in} > 420V: no operation	Normal operation is entered with soft-start

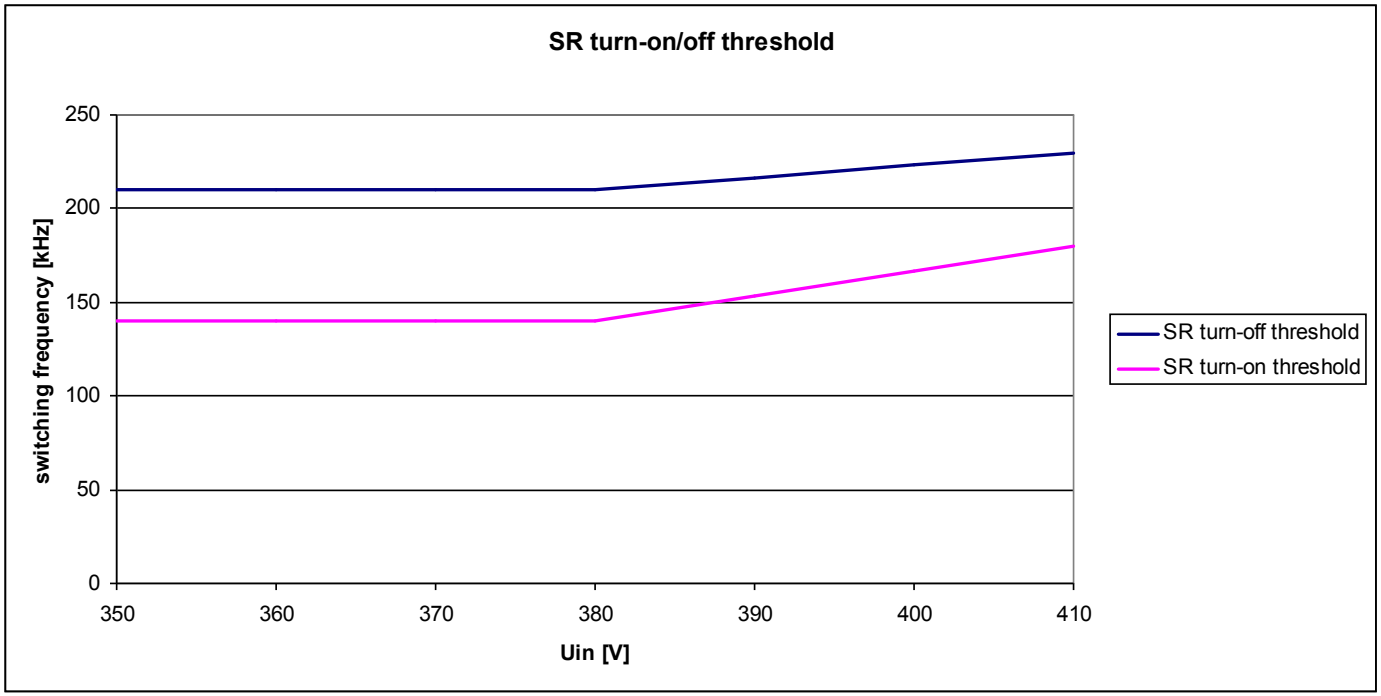
Functional Description – SR Control

Feature	Concept of implementation	Remark
SR softstart	1. Initial duty cycle of 0% 2. Step by step Increase to full duty cycle	
SR on/off control	SR is turned on if **all** conditions are true: • U_{freq} > 1.138V @Uin=380V (threshold depending on input voltage) • U_{cs} < 0.54V • Elapsed time since soft-start finished > 20ms • Elapsed time since over current protection > 10ms SR is turned off is **one** condition is true: • U_{freq} < 0.605V @Uin=380V (threshold depending on input voltage) • U_{cs} > 0.82 • during over current protection • Soft-start active	
On-time control	On-time is set in dependence of input voltage and switching frequency. Once estimated by experiment the values for SR on-times are saved in a table.	
Turn-on delay	If V_{in} is higher than resonant voltage (set by define directive) a turn-on delay of 250ns is added (SR Gate is turned on 250ns after the corresponding primary gate) Turn-on delay is realized with phase shift between primary and secondary PWM signals	
Turn-off delay	In current design turn-off delay is not needed because of use of fast optocoupler for SR gate signals	

Voltage Controlled Oscillator



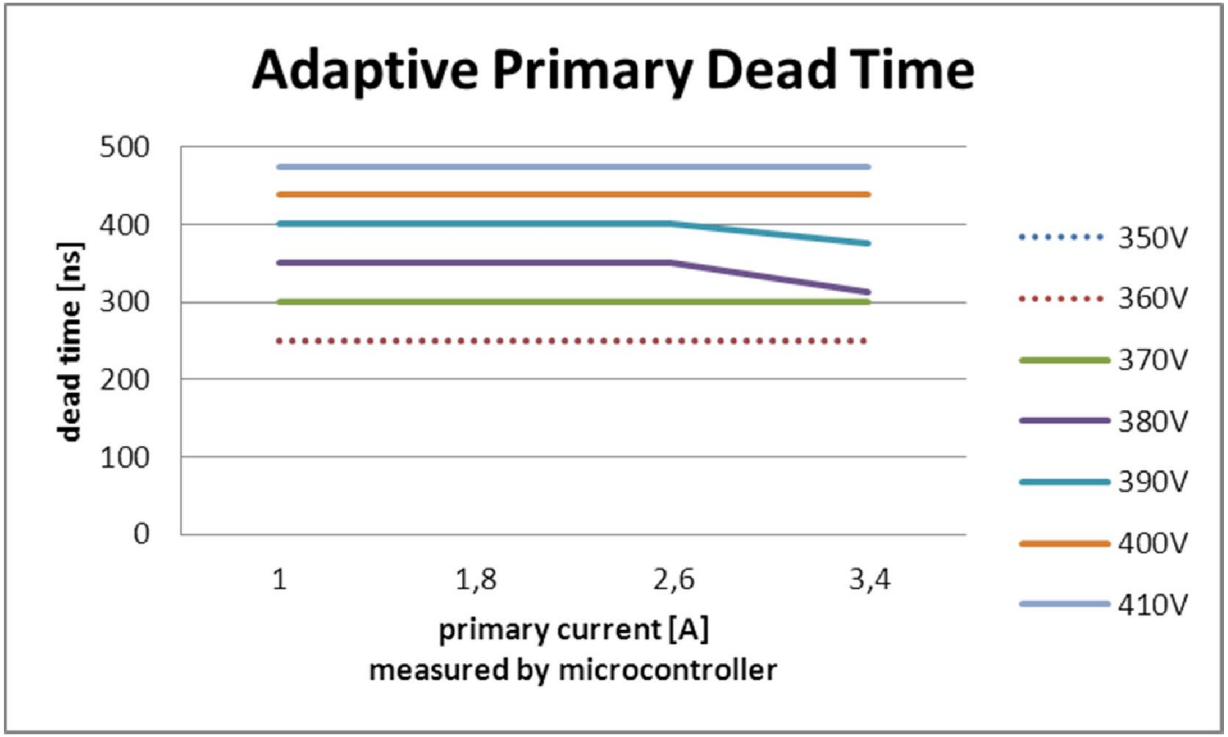
SR turn-on/off threshold



Optimized SR turn-on/off thresholds in dependence of input voltage are implemented:

- If the input voltage increases the switching frequency also increases (assuming constant output current)
- To turn-on and off the SR at the same output current the turn-on/off thresholds have to be adapted

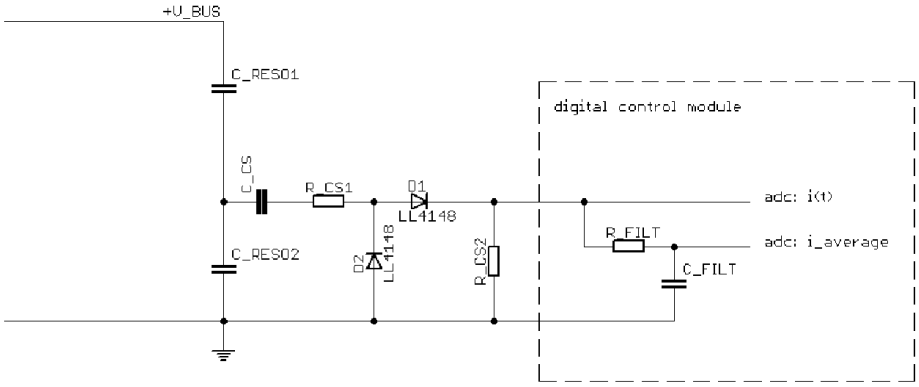
Adaptive primary dead time



The primary dead time is changed in accordance to input vontage and input current.

Functional Description – anti cap mode

- For detection of capacitive mode the instantaneous resonant current must be measured



- Conversion of adc is synchronized with rising edge of the highside MOSFET pwm signal
  - A voltage higher than 0.2V is a clear indication for capacitive mode operation
  - In this case the converter will switch of and resume operation with soft start

Software Test Procedure and Documentation

- Verification of software by application test
  - Digital controlled llc converter has to meet at least the same requirements than the analog controlled version
  - Test report with following items is applied (referred to the existing document):
    - Line/load regulation
    - Output voltage ripple
    - Protections (OVP, OCP, sort circuit)
    - Dynamic load-transient response
    - Oscilloscope plots including most significant waveforms
    - Efficiency plot
- No software module tests are applied
- No specific software test report is required

- Software documentation
  - Creation of documentation files by Doxygen (source: www.doxygen.org)
  - C-source code will contain comments readable for Doxygen parser
  - Flow chart of state machine is provided